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DESIGN AND SIMULATION OF VEDIC DIVIDER USING REVERSIBLE LOGIC

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Abstract— Low power consumption, high speed and smaller area are some of the most important aspects for the designing of any VLSI system. Area and speed are usually incompatible constraints so good design has to set the equilibrium between area and speed. Through work in this paper we try to determine the best solution to this problem. Vedic algorithm is most popularly used ancient algorithm which yields quicker results by using basic addition and multiplication technique. Vedic mathematics consists of 16 sutras. It covers explanation of several modern arithmetical terms. In this project various Vedic sutras are used for all type of reversible division process. To design circuit VHDL coding will be used (Very High Speed Integrated Circuits Hardware Description Language) by combining Boolean logic with ancient Vedic mathematical technique for obtaining high speed divisor for improving speed.

Keywords— Vedic Mathematics, Nikhilam Navatascaramam Dashatah, Vhdl Code.

I. INTRODUCTION

Many recursive techniques have so far been proposed by various researchers to implement the high speed divider [1-10], such as digit recurrence implementation methodology (restoring, non-restoring, division by convergence method Newton-Raphson method [10], division by series expansion (Goldschmidt algorithm) [10]. The cost in terms of area and computational complexity of digit recurrence algorithms is low due to the large number of iterations therefore; latency (propagation delay) becomes high. While, some of the investigator relies on higher radix implementation of digit recurrence algorithm to reduce the iteration, therefore the latency becomes improved from the earlier reports, but this scheme additionally increases the hardware complexity.

Some other attractive ideas are based on functional iterations, like Newton-Raphson and Goldschmidt's algorithm, that utilize multiplication techniques along with the series expansion, where the amount of quotient digits obtained per iteration is doubled[10]. The drawback of these methods is operands should be previously normalized, most used primitive are multiplications, and the remainder is not directly obtained. In algorithmic and structural levels, a lot of division techniques had been developed to reduce the latency of the divider circuitry; which reduces the iteration aiming to reduction of latency but the principle behind division was same in all cases. Vedic Mathematics is the ancient system of Indian mathematics which is based on 16 Sutras (Formulae) has a unique technique of calculations.

1.1 Vedic Mathematics

The uses of Vedic Mathematics shows its application in fast calculations (multiplication, division, squaring, cubing, square root, cube root), three-dimensional coordinate geometry, trigonometry, linear and non-linear differential equations, solution of plane and spherical triangles, matrices and determinants, log and exponential[4]. The most interesting point is to note that the Vedic Mathematics provides unique solutions where trial and error method is available at present. Vedic Mathematics offers a fresh and highly efficient approach to mathematics covering a wide range - starts with elementary multiplication and concludes with a relatively advanced topic, the solution of non-linear partial differential equations [4-5]. But the Vedic scheme is not simply a collection of a fast calculation methods; it is a system, a unified approach. Vedic Mathematics extensively exploits the properties of numbers in every practical application. Using these Vedic techniques various arithmetic modules can be designed and integrated into a Vedic ALU, which is compatible for Co-Processors. This Vedic Co-Processor will be more efficient than the conventional one.

1.2 Vedic Sutra

The gifts of the ancient Indian mathematics in the world history of mathematical science are not well recognized. The contributions of mathematician in the field of number theory, 'Sri Bharati Krsna Thirthaji Maharaja', in the form of Vedic Sutras (formulae) [15] are significant for calculations. He had explored the mathematical potentials from Vedic primers and showed that the mathematical operations can be carried out mentally using the Sutras (Formulae) to produce fast answers. In this paper we report only NND formula to implement the division algorithm and its architecture.

"Nikhilam Navatascaramam Dasatah" (NND) is a Sanskrit term i.e. "all from 9 and last from 10", formula have been mathematically described for the proposed design.

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II. LITERATURE REVIEW

Rakshith Saligram, Rakshith T.R ," Optimized Reversible Vedic Multipliers for High Speed Low Power Operations"

In this paper reversible Urdhva-Tiryakbhyam sutra is used. This is better in both speed and power. The focus of this paper is mainly to design a low power high speed multiplier design which is implemented by constructing the multiplier using reversible logic gates. The minimum improvement in the total reversible logic implementation cost (TRLIC) is at 5.86% which is w.r.to and the maximum improvement stand high at33.6%.

Asmita Haveliya " FPGA implementation of a vedic convolution algorihm"

In this paper, Urdhva-Tiryakbhyam sutra is used. It is seen that there is a considerable improvement in the performance of the multiplier in vedic multiplication for OLA . Total real time to Xst completion is 775.00secs and total CPU time to Xst completion is 774.89secs. Total memory usage is 317328 kilobytes.

Prabir Saha, Arindam Banerjee, Partha Bhattacharyya, Anup Dandapat, "Vedic Divider: Novel Architecture (ASIC) for High Speed VLSI Application"

In this paper, "Nikhilam Navatascaramam Dasatah" sutra is used. Prorogation delay and dynamic power consumption of a divider circuitry were minimized significantly by removing unnecessary recursion through Vedic division methodology. The prorogation delay of the resulting 16-bit binary dividend by an 8-bit divider circuitry was only 10.5ns and consumed 24uW power for layout area of 10.25m[illegible]

III. PROBLEM DEFINATION

In Urdhva-Tiryakbhyam sutra, large number of multiplication and addition is preformed therefore hardware required is more.

As the number of hardware is increased, speed reduces.

IV. OBJECTIVE

Design the reversible divisor using "Nikhilam Navatascaramam Dasatah" sutra (All from 9 and last from 10).

Due to the use of NND division sutra number of hardware required in the circuit reduces which improves the speed of the divisor.

V. METHODOLOGY AND CONCLUSION

Nikhilam Navatascaramam Dashatah Sutra for Division

Example 1: Consider the division 1235 / 89.
Conventional method:

```
89) 1235 ( 13
89____
  345
  267
 ____
   78
```

Thus Q = 13 and R = 78.
Fast Math's method:
This method is useful when the divisor is nearer and Less than the base. Since for 89, the base is 100 therefore this method can be applied.

Step (i): Write the dividend and divisor as in the conventional method. Obtain the modified divisor (M.D.) by applying the complement formula. Write M.D. just below the actual divisor. Thus for the divisor 89, the M.D. obtained by using complement is 11 in the "all from 9 and last from 10 method".
Now Step 1 gives

```
89) 1235
11
```

Step (ii): Bifurcate the dividend by a slash so that RHS of dividend contains the number of digits equal to that of M.D. Here M.D. contains 2 digits hence

```
89 ) 12 / 35
11
```

Step (iii): Multiply the M.D. with first column digit of the dividend. Here it is 1. i.e.

11 x 1 =11. Write this product place wise under the 2nd and 3rd columns of the dividend.

```
89 ) 12/3 5
11    1 1
      1
```

Step (iv): Add the digits in the 2nd column and multiply the M.D. with that result i.e. 2+1=3 and 11x3=33. Write the digits of this result column wise as shown below, under 3rd and 4th columns. i.e.

```
89 ) 12/3 5
11    1 1
        3 3
      13 /
```

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Step (v): Add the digits in the 3rd column 3+1 +3=7. Add the digits in the 4th column 5+3 =8.

89) 12 /3 5
11 1 1
3 3
13/7 8

Now the division process is complete, giving Q= 13 and R = 78.

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